ABSTRACT OF THE DISCLOSURE

Relates to automatic conversion of assumption constraints, used in circuit design verification, that model an environment for testing a DUT/DUV, where the assumptions specify sequential behavior.

5 Such assumptions are converted, with the use of logic synthesis tools, into a gate-level representation.

For formal verification, a verification output is constructed from the gate-level representation and DUT/DUV assertion-monitoring circuitry. A formal verifier seeks to prove the verification output cannot indicate a design error.

10 For simulation verification, the gate-level representation is converted into a hybrid representation comprising pipelines and combinational constraints. During simulation, the pipelines hold state information necessary for a solution, of the combinational constraints, to be in accord with the sequential assumption constraints.

15 For certain sequential assumption constraints, the combinational constraints are insufficient to insure avoidance of deadend states. In a deadend state, an assumption is violated.

A method is presented for augmenting the combinational constraints to avoid deadend states.

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